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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,881	03/31/2004	Masahiro Koyama	500.37600CX1	4560
24956 7590 08/20/2007 MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C. 1800 DIAGONAL ROAD SUITE 370 ALEXANDRIA, VA 22314			EXAMINER LAFORGIA, CHRISTIAN A	
			ART UNIT 2131	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/812,881

Applicant(s)

KOYAMA ET AL.

Examiner

Christian La Forgia

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 March 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☒ Certified copies of the priority documents have been received in Application No. 09/398,776.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>3/31/04;3/16/05</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-21 have been presented for examination.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 09/398,776, filed on 20 September 1999.

Information Disclosure Statement

3. The information disclosure statements (IDS) submitted on 16 March 2005 and 31 March 2004 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the examiner has considered the information disclosure statement.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 17-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The term "substantially" in claims 17-21 is a relative term which renders the claim indefinite. The term "substantially" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. See MPEP § 2173.05(b); see also *In re Nehrenberg*, 280 F.2d 161, 126 USPQ 383 (CCPA 1960).

Claim Rejections - 35 USC § 101

6. 35 U.S.C. 101 reads as follows:

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Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

7. Claims 15, 16, and 21 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. As per claims 15, 16, and 21, merely claimed as a computer program representing a computer listing *per se*, that is, descriptions or expressions of such a program and that is, descriptive material *per se*, non-functional descriptive material, and is not statutory because it is not a physical “thing” nor a statutory process, as there are not “acts” being performed. Such claimed computer programs do not define any structural and functional interrelationships between the computer program and other claimed aspects of the invention which permit the computer program’s functionality to be realized. Since a computer program is merely a set of instructions capable of being executed by a computer, the program itself is not a process, without the computer-readable medium needed to realize the computer program’s functionality. In contrast, a claimed computer-readable medium encoded with a computer program defines structural and functional interrelationships between the computer program and the medium which permit the computer program’s functionality to be realized, and is thus statutory. **Warmerdam**, 33 F.3d at 1361, 31 USPQ2d at 1760. **In re Sarkar**, 588 F.2d 1330, 1333, 200 USPQ 132, 137 (CCPA 1978). See MPEP § 2106(IV)(B)(1)(a).

8. Claims 15, 16, and 21 are directed to a computer program to be executed. This is construed as being capable of being executed, but not necessarily in the act of being executed. Since the program is not claimed as being executed or embodied on a computer-readable recording medium, it merely represents a computer listing *per se*.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claims 1, 3-7, and 9-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,370,560 B1 to Robertazzi et al., hereinafter Robertazzi, in view of U.S. Patent No. 5,978,831 to Ahamed et al, hereinafter Ahamed.

11. As per claim 1, Robertazzi teaches a decentralized control system, comprising:

a plurality of processors (Figures 1a [blocks 105, 107, 109], 1c [block 181], 5, 6, 8; column 2, lines 55-60; column 3, lines 55-60; column 5, lines 29-40);

a plurality of devices controlled by said plurality of processors (column 5, lines 33-44);
and,

at least one information transmission path for communicating control of information between the plurality of processors and for communicating input/output information between said plurality of processors and the devices (Figures 1 [blocks 121, 123, 125], 3 [block 313]; column 5, line 62 to column 6, line 4; column 10, line 23-38);

at least one of the plurality of processors comprising:

processor detecting means for detecting a connection state of each of the plurality of processors with respect to the information transmission path, said connection state being represented by an ID of each of said processors (Figures 1c [block 183], 2a [block 205]; column 6, lines 44-46; column 8, lines 33-50);

program block assigning means for assigning, based on the detected connection state detected by said processor detecting means, a plurality of mutually concurrently executable program blocks to control the device to each of the plurality of processors, respectively, said assigning means dividing a program for controlling said devices into said mutually concurrently executable plurality of blocks, and said assigning means distributing said mutually concurrently executable plurality of blocks to said processors (Figures 1a & 1b [block 103], 2c [block 217], 4 [block 409], 7 [block 703, 705, 707, 709]; column 2, lines 52-60; column 5, lines 26-30; column 6, lines 11-14; column 6, line 67 to column 7, line 23; column 8, lines 44-60; column 12, lines 3-13; column 13, lines 28-50); and

a program storage means for storing a relevant one of the plurality of mutually concurrently executable program blocks at each of the plurality of processors, each of the plurality of processors executing the stored relevant program blocks, respectively (Figure 1a [block 111], 1b [block 115]; column 5, lines 52-61).

Wherein the plurality of devices is drawn to memory and other features found on common computer systems, as well as the proprietary software and hardware enhancements discussed in Robertazzi. Wherein the connection state is drawn to whether the processor is “busy” or “available.”

12. Robertazzi does not teach uniformly assigning a processing load to processors in accordance with an average number of execution steps or an average processing time for one cycle of each of the plurality of program blocks.

13. Ahamed discloses a method of distributing portions of a received task to individual processors in portions that are directly proportional in size to their operating rate, thereby performing their respective tasks in the same amount of time (Abstract, column 2, lines 15-29), which is drawn to the Applicant's claimed assignment of processing loads based on an average processing time for one cycle of each of the plurality of program blocks.

14. It would have been obvious to one of ordinary skill in the art at the time the invention was made to uniformly assigning a processing load to processors in accordance with an average number of execution steps or an average processing time for one cycle of each of the plurality of program blocks, since Ahamed states at column 3, lines 46-49 that the aforementioned scheduling technique allows for the construction of very high-speed pipelined processors without the need to construct them from very high-cost, high-speed uniprocessor stages

15. Regarding claim 3, Robertazzi teaches each of the plurality of processors detects by the processor detecting means thereof available processors connected to the information transmission path and assigns by the program assigning means thereof processing of the program blocks respectively to the plurality of processors (Figures 1c [block 183], 2a [block 205]; column 6, lines 44-46; column 8, lines 33-50).

16. Regarding claim 4, Robertazzi teaches either one of the plurality of processors generates by the program block assigning means an allocation table in which the program blocks are subdivided into several groups to be respectively assigned to the plurality of processors to possibly uniformly assign a processing load to the processors in accordance with an average

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number of steps or an average processing time for one cycle of each of the plural program blocks and sends the table to each of the plurality of processors together with all the program blocks (column 6, lines 11-14; column 6, lines 39-65). Robertazzi and Ahamed do not teach sending the table to each of the plurality of processors. Robertazzi does disclose making the table available to all of the processors via a central file server or a web site in column 6. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to transfer the table to the plurality of processors. One would be motivated to provide for this information in order to reallocate a task or load, as described in Figures 2b, 4, and 7.

17. With regards to claim 5, Robertazzi teaches either one of the plurality of processors subdivides by the program block assigning means the program blocks into program block sets each including several ones of the program blocks and assigns the program block sets respectively to the plurality of processors to possibly uniformly assign a processing load to the processors in accordance with an average number of steps or an average processing time for one cycle of each of the plurality of program blocks and sends the program block sets respectively to the plurality of processors (Figures 1a & 1b [block 103], 2c [block 217], 4 [block 409], 7 [block 703, 705, 707, 709]; column 2, lines 52-60; column 5, lines 26-30; column 6, lines 11-14; column 6, line 67 to column 7, line 23; column 8, lines 44-60; column 12, lines 3-13; column 13, lines 28-50).

18. Regarding claim 6, Robertazzi teaches a means for generating, in accordance with connection states sent via the information transmission path from other processors, a list of

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available processors connected to the information transmission path (Figures 1c [block 183], 2a [block 205]; column 6, lines 44-46; column 8, lines 33-50);

means for multicasting via the information transmission path a connection state of its own processor with respect to the information transmission path, the means including the processor detecting means (column 6, lines 11-14; column 6, lines 39-65). Robertazzi does not teach multicasting processor availability. Robertazzi does disclose making processor availability available to all of the processors via a central file server or a web site in column 6. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to multicast the availability of the plurality of processors to all of the processors. One would be motivated to provide for this information in order to reallocate a task or load, as described in Figures 2b, 4, and 7.

19. Regarding claim 7, Robertazzi teaches that either one of the plurality of processors detects by the processor detecting means, when the connection state of either one of said plurality of processors is changed in the decentralized control system or either one of the plurality of processors fails when the decentralized control system is in operation, available processors and assigns by the program block assigning means processing of the plural program blocks to the available processors (Figures 1c [block 183], 2a [block 205]; column 6, lines 44-46; column 8, lines 33-50).

20. As per claim 9, Robertazzi teaches a decentralized control system network, comprising:

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a plurality of processors (Figures 1a [blocks 105, 107, 109], 1c [block 181], 5, 6, 8; column 2, lines 55-60; column 3, lines 55-60; column 5, lines 29-40);

at least one device controlled by the plurality of processors (column 5, lines 33-44); and,
at least one information transmission path for communicating control of information between the plural processors and for communicating input/output information between the plurality of processors and the device (Figures 1 [blocks 121, 123, 125], 3 [block 313]; column 5, line 62 to column 6, line 4; column 10, line 23-38), wherein

at least one of the plurality of processors includes:

processor detecting means for detecting a connection state of each of the plurality of processors with respect to the information transmission path, the connection state showing which processors of said plurality of processors are connected for controlling the at least one device (Figures 1c [block 183], 2a [block 205]; column 6, lines 44-46; column 8, lines 33-50);

program block assigning means responsive to an output from the processor detecting means for assigning, based on the detected connection state from the processor detecting means, a plurality of mutually concurrently executable program blocks to control the device respectively to available ones of the plurality of processors (Figures 1a & 1b [block 103], 2c [block 217], 4 [block 409], 7 [block 703, 705, 707, 709]; column 2, lines 52-60; column 5, lines 26-30; column 6, lines 11-14; column 6, line 67 to column 7, line 23; column 8, lines 44-60; column 12, lines 3-13; column 13, lines 28-50); and

a program storage means for storing a relevant one of the plurality of mutually concurrently executable program blocks at the respective available ones of the plurality

of processors, the respective available ones of the plurality of processors executing the stored relevant program block (Figure 1a [block 111], 1b [block 115]; column 5, lines 52-61).

21. Robertazzi does not teach uniformly assigning a processing load to processors in accordance with an average number of execution steps or an average processing time for one cycle of each of the plurality of program blocks.

22. Ahamed discloses a method of distributing portions of a received task to individual processors in portions that are directly proportional in size to their operating rate, thereby performing their respective tasks in the same amount of time (Abstract, column 2, lines 15-29), which is drawn to the Applicant's claimed assignment of processing loads based on an average processing time for one cycle of each of the plurality of program blocks.

23. It would have been obvious to one of ordinary skill in the art at the time the invention was made to uniformly assigning a processing load to processors in accordance with an average number of execution steps or an average processing time for one cycle of each of the plurality of program blocks, since Ahamed states at column 3, lines 46-49 that the aforementioned scheduling technique allows for the construction of very high-speed pipelined processors without the need to construct them from very high-cost, high-speed uniprocessor stages

24. Regarding claim 10, Robertazzi teaches each of the processors includes a state transmitting means for transmitting, in place of the processor detecting means, information indicative of whether or not its own processor is available in the system to the transmission path (column 8, lines 44-50).

25. As per claim 11, Robertazzi teaches an operation method for use with a decentralized control system network including a plurality of processors, a plurality of devices controlled by the plurality of processors, and at least one information transmission path for communicating control information between the plural processors and for communicating input/output information between the plurality of processors and the device, comprising:

detecting by at least one of the plurality of processors a connection state of each of the plural processors with respect to the information transmission path, said connection state being represented by an ID of each of said processors and showing which processors of said plurality of processors are connected for controlling the plurality of devices (Figures 1c [block 183], 2a [block 205]; column 6, lines 44-46; column 8, lines 33-50);

assigning, in response to a detection result from the processor detecting step, and based on the detected connection state, a plurality of mutually concurrently executable program blocks to control the device respectively to the plurality of processors, respectively (Figures 1a & 1b [block 103], 2c [block 217], 4 [block 409], 7 [block 703, 705, 707, 709]; column 2, lines 52-60; column 5, lines 26-30; column 6, lines 11-14; column 6, line 67 to column 7, line 23; column 8, lines 44-60; column 12, lines 3-13; column 13, lines 28-50), said assigning including:

dividing a program for controlling said devices into said mutually concurrently executable plurality of blocks (column 2, lines 52-60; column 3, lines 55-66; column 4, lines 7-13); and,

distributing the mutually concurrently executable program blocks to said devices to be controlled (column 2, lines 52-60; column 3, lines 55-66; column 4, lines 7-13);

storing the mutually concurrently executable program blocks in the available processors, respectively (Figure 3 [block 303]; column 10, lines 38-59).

Wherein the plurality of devices is drawn to memory, resources, and other features found on common computer systems, as well as the proprietary software and hardware enhancements discussed in Robertazzi. Wherein the connection state is drawn to whether the processor is “busy” or “available.”

26. Robertazzi does not teach uniformly assigning a processing load to processors in accordance with an average number of execution steps or an average processing time for one cycle of each of the plurality of program blocks.

27. Ahamed discloses a method of distributing portions of a received task to individual processors in portions that are directly proportional in size to their operating rate, thereby performing their respective tasks in the same amount of time (Abstract, column 2, lines 15-29), which is drawn to the Applicant’s claimed assignment of processing loads based on an average processing time for one cycle of each of the plurality of program blocks.

28. It would have been obvious to one of ordinary skill in the art at the time the invention was made to uniformly assigning a processing load to processors in accordance with an average number of execution steps or an average processing time for one cycle of each of the plurality of program blocks, since Ahamed states at column 3, lines 46-49 that the aforementioned scheduling technique allows for the construction of very high-speed pipelined processors without the need to construct them from very high-cost, high-speed uniprocessor stages

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29. Regarding claim 12, Robertazzi teaches including in place of the processor detecting step of each of the processors, a step of transmitting to the transmission path an indication whether or not its own processor is available in the system (column 8, lines 44-50).

30. As per claim 13, Robertazzi teaches a computer-readable recording media for storing thereon a program executable by a computer an operation method for use with a decentralized control system network including:

a plurality of processors (Figures 1a [blocks 105, 107, 109], 1c [block 181], 5, 6, 8; column 2, lines 55-60; column 3, lines 55-60; column 5, lines 29-40);

at least one device controlled by the plurality of processors (column 5, lines 33-44); and,

at least one information transmission path for communicating control of information between the plurality of processors and for communicating input/output information between the plurality of processors and the device (Figures 1 [blocks 121, 123, 125], 3 [block 313]; column 5, line 62 to column 6, line 4; column 10, line 23-38), the program comprising:

detecting by at least one of the plural processors a connection state of each of the plurality of processors with respect to the information transmission path, the connection state showing which processors of said plurality of processors are connected for controlling the at least one device (Figures 1c [block 183], 2a [block 205]; column 6, lines 44-46; column 8, lines 33-50); and,

assigning, in response to a detection result from the processor detecting step, and based on the detected connection state, a plurality of mutually concurrently executable program blocks to control the device to available ones of the plurality of processors, respectively (Figures 1a &

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1b [block 103], 2c [block 217], 4 [block 409], 7 [block 703, 705, 707, 709]; column 2, lines 52-60; column 5, lines 26-30; column 6, lines 11-14; column 6, line 67 to column 7, line 23; column 8, lines 44-60; column 12, lines 3-13; column 13, lines 28-50);

storing the assigned mutually concurrently executable program blocks in the available processors, respectively (Figure 3 [block 303]; column 10, lines 38-59). Wherein the plurality of devices is drawn to memory and other features found on common computer systems, as well as the proprietary software and hardware enhancements discussed in Robertazzi. Wherein the connection state is drawn to whether the processor is “busy” or “available.”

31. Robertazzi does not teach uniformly assigning a processing load to processors in accordance with an average number of execution steps or an average processing time for one cycle of each of the plurality of program blocks.

32. Ahamed discloses a method of distributing portions of a received task to individual processors in portions that are directly proportional in size to their operating rate, thereby performing their respective tasks in the same amount of time (Abstract, column 2, lines 15-29), which is drawn to the Applicant’s claimed assignment of processing loads based on an average processing time for one cycle of each of the plurality of program blocks.

33. It would have been obvious to one of ordinary skill in the art at the time the invention was made to uniformly assigning a processing load to processors in accordance with an average number of execution steps or an average processing time for one cycle of each of the plurality of program blocks, since Ahamed states at column 3, lines 46-49 that the aforementioned scheduling technique allows for the construction of very high-speed pipelined processors without the need to construct them from very high-cost, high-speed uniprocessor stages

34. Regarding claim 14, Robertazzi teaches the program further including, in place of the detecting step, a step of transmitting to the transmission path an indication whether or not its own processor is available (column 8, lines 44-50).

35. As per claim 15, Robertazzi teaches for a decentralized control system network including:

a plurality of processors (Figures 1a [blocks 105, 107, 109], 1c [block 181], 5, 6, 8; column 2, lines 55-60; column 3, lines 55-60; column 5, lines 29-40);

at least one device controlled by the plurality of processors (column 5, lines 33-44); and,

at least one information transmission path for communicating control of information between the plurality of processors and for communicating input/output information between the plurality of processors and the device (Figures 1 [blocks 121, 123, 125], 3 [block 313]; column 5, line 62 to column 6, line 4; column 10, line 23-38), a program to be used by at least one of the plurality of processors executes the following steps of:

detecting in at least one of the plurality of processors a connection state of each of the plurality of processors with respect to the information transmission path, the connection state showing which processors of said plurality of processors are connected for controlling the devices (Figures 1c [block 183], 2a [block 205]; column 6, lines 44-46; column 8, lines 33-50);

assigning, in response to a detection result from the processor detecting step, and based on the detected connection state, a plurality of mutually concurrently executable program blocks to control the device to available ones of the plural processors, respectively (Figures 1a & 1b

[block 103], 2c [block 217], 4 [block 409], 7 [block 703, 705, 707, 709]; column 2, lines 52-60; column 5, lines 26-30; column 6, lines 11-14; column 6, line 67 to column 7, line 23; column 8, lines 44-60; column 12, lines 3-13; column 13, lines 28-50);

storing the assigned mutually concurrently executable program blocks in the available processors, respectively (Figure 3 [block 303]; column 10, lines 38-59). Wherein the plurality of devices is drawn to memory and other features found on common computer systems, as well as the proprietary software and hardware enhancements discussed in Robertazzi. Wherein the connection state is drawn to whether the processor is “busy” or “available.”

36. Robertazzi does not teach uniformly assigning a processing load to processors in accordance with an average number of execution steps or an average processing time for one cycle of each of the plurality of program blocks.

37. Ahamed discloses a method of distributing portions of a received task to individual processors in portions that are directly proportional in size to their operating rate, thereby performing their respective tasks in the same amount of time (Abstract, column 2, lines 15-29), which is drawn to the Applicant’s claimed assignment of processing loads based on an average processing time for one cycle of each of the plurality of program blocks.

38. It would have been obvious to one of ordinary skill in the art at the time the invention was made to uniformly assigning a processing load to processors in accordance with an average number of execution steps or an average processing time for one cycle of each of the plurality of program blocks, since Ahamed states at column 3, lines 46-49 that the aforementioned scheduling technique allows for the construction of very high-speed pipelined processors without the need to construct them from very high-cost, high-speed uniprocessor stages

39. Regarding claim 16, Robertazzi teaches in place of the detecting step of each of the processors, a step of transmitting to the transmission path an indication whether or not its own processor is available (column 8, lines 44-50).

40. Regarding claims 17-21, Ahamed teaches wherein each of numbers of instructions of the mutually concurrently executable program blocks to be assigned to each of the processors are made substantially equal (column 3, lines 22-66, i.e. distributing data in portions that are directly proportional to the processors operating rate).

41. Claims 2 and 8 are rejected under 35 U.S.C. 103(a) as being obvious over Robertazzi in view of Ahamed as applied above, and further in view of United States Patent No. 5,592,671 to Hirayama, hereinafter Hirayama.

42. Regarding claim 2, Robertazzi does not teach a particular processor selected in accordance with the priority level from available processors detected by the processor detecting means assigns by the program assigning means processing of the program blocks respectively to said plurality of processors;

the plurality of processors are assigned with priority levels beforehand.

43. Hirayama teaches a particular processor selected in accordance with the priority level from available processors detected by the processor detecting means assigns by the program assigning means processing of the program blocks respectively to said plurality of processors (Figures 1, 5, 8; column 3, lines 17-34; column 3, lines 43-57);

the plurality of processors are assigned with priority levels beforehand (column 3, lines 27-30). Robertazzi suggests in column 5 that the plurality of processors rank differently amongst themselves, particularly amongst processing power and speed. Furthermore, Robertazzi discloses running the divisible task on slower machines, that will take longer and cost less or executing the divisible task on faster processors, costing more, but taking less time in columns 10 and 11. Therefore it would have been obvious to one of ordinary skill in the art, with a working knowledge of Hirayama, at the time the invention was made to assign a priority level to each of the plurality of processors.

44. Regarding claim 8, Robertazzi does not the information transmission path includes two channels, namely, a control information transmission path for communicating the control information and an input/output information transmission path to communicate the input/output information.

45. Hirayama teaches the information transmission path includes two channels, namely, a control information transmission path for communicating the control information and an input/output information transmission path to communicate the input/output information (Figures 5 [blocks 53, 520, 521, 522, 52n], 7 [blocks 73, 702, 712, 722, 7m2]; column 4, line 64 to column 5, line 9; column 6, line 54 to column 7, line 4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have two channels, an I/O path and a control path, in the system of Saito. One would be motivated to include these multiple channels for redundancy purposes. In the case that a processor fails and control has to be transferred to another processor, the other processors can communicate without putting traffic on

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the I/O path and disrupting that path. Likewise, if a processor fails, the information on the I/O path can just be forwarded to the appropriate processor without having to retransmit the information several times until it finds the appropriate processor.

Conclusion

46. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christian La Forgia whose telephone number is (571) 272-3792. The examiner can normally be reached on Monday thru Thursday 7-5.

47. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ayaz Sheikh can be reached on (571) 272-3795. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

48. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Christian LaForgia
Patent Examiner
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A handwritten signature in black ink, appearing to read 'CLF', with a large, stylized loop at the bottom.

clf